

FIG. 2

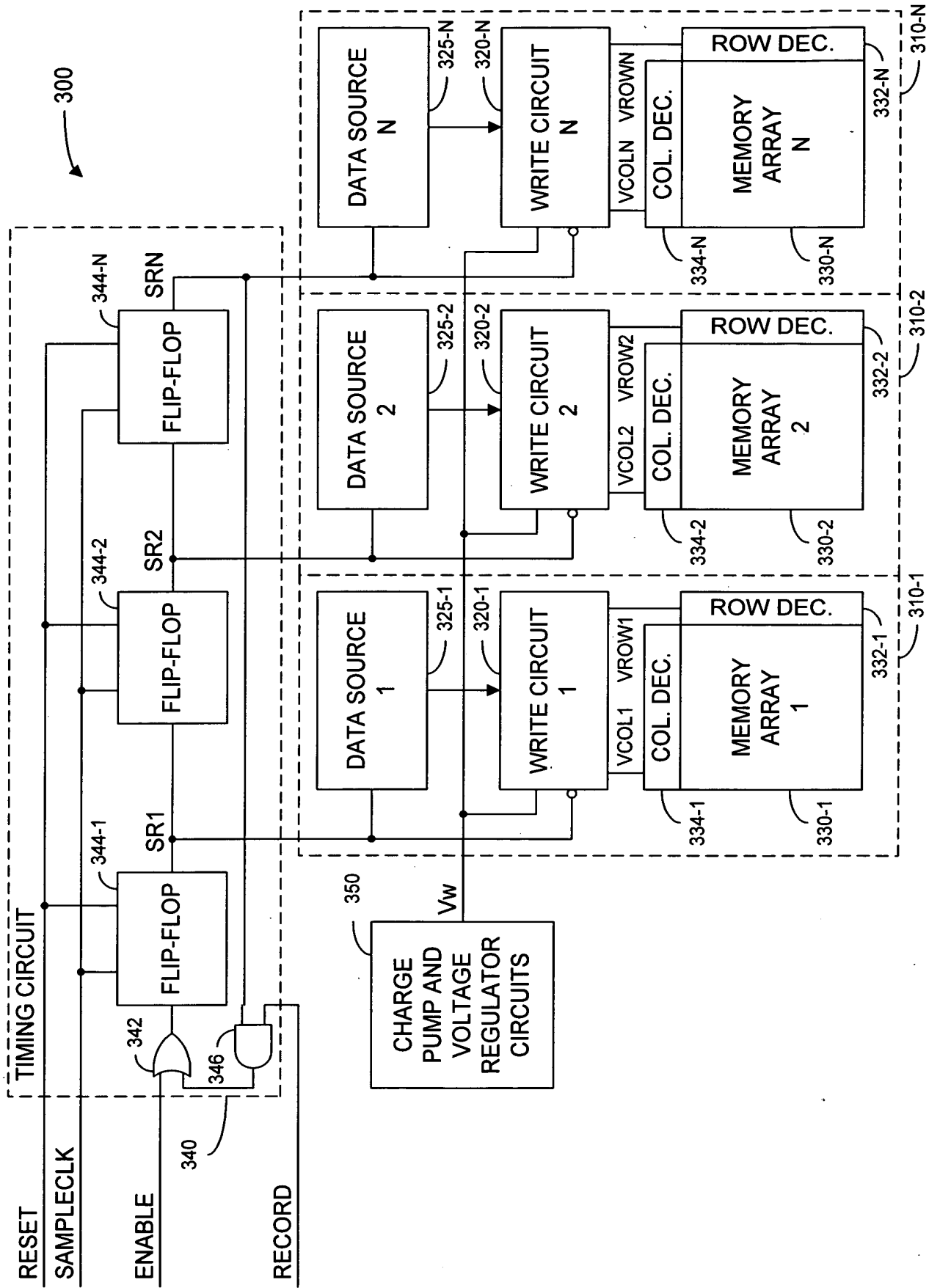


FIG. 3

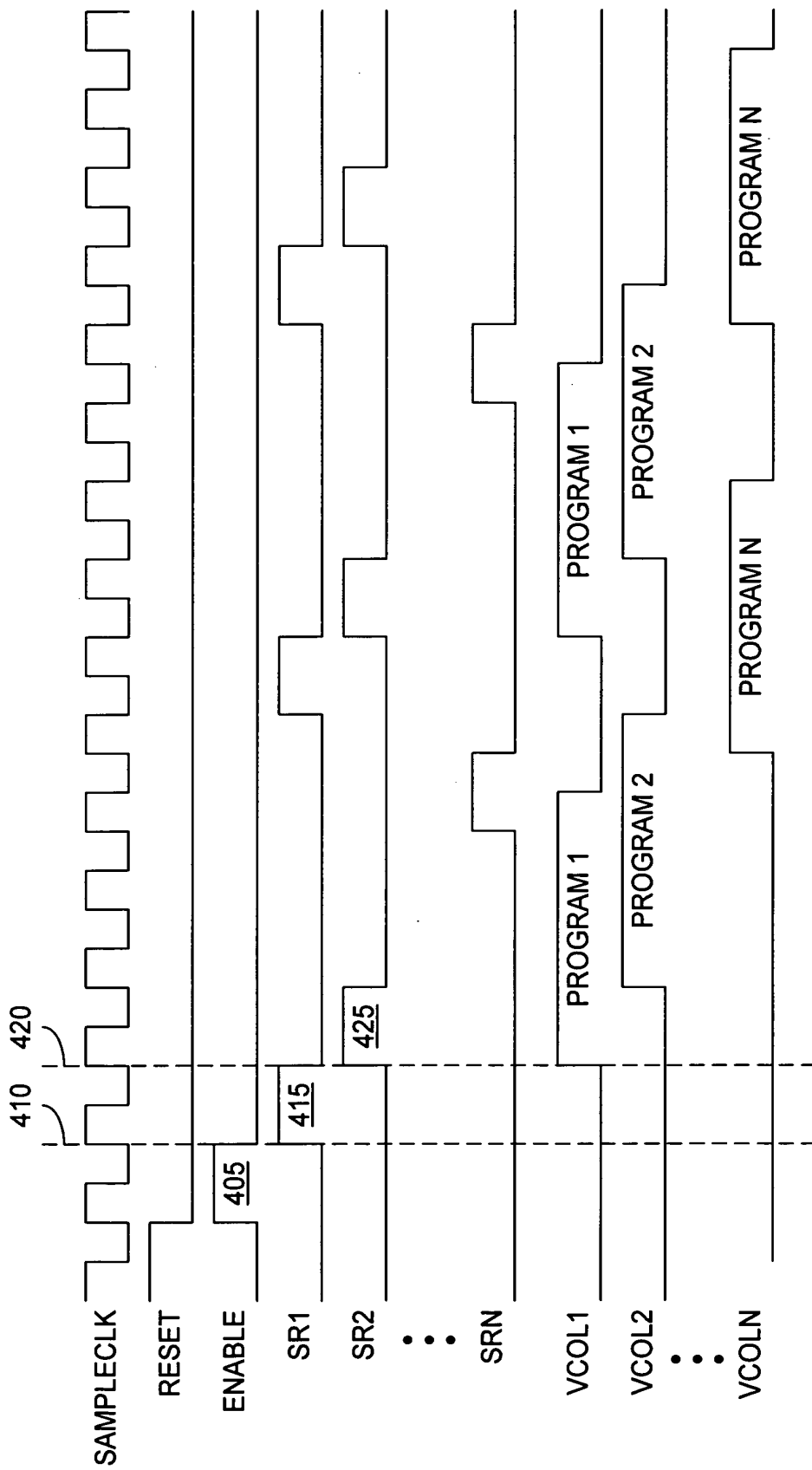


FIG. 4

FIG. 5

The timing diagram illustrates the relationship between several signals over time, with specific intervals marked by dashed lines and labels 610, 620, 630, 640, and 650. The signals are:

- SAMPLECLK**: A periodic square wave clock signal.
- RESET**: A single high pulse.
- ENABLE**: A single high pulse labeled 605.
- SR1**: A signal pulse labeled 615.
- SR2**: A signal pulse labeled 625.
- SRN**: A signal pulse labeled 645.
- VCOL1**: A signal that transitions from a low level to a high level labeled $-V_w$, then to a lower high level labeled $-V_r$.
- I1**: A signal that transitions from a low level to a high level labeled $-V_w$, then to a lower high level labeled $-V_r$.
- VCOL2**: A signal that transitions from a low level to a high level labeled $-V_w$, then to a lower high level labeled $-V_r$.
- I2**: A signal that transitions from a low level to a high level labeled $-V_w$, then to a lower high level labeled $-V_r$.

The diagram shows that the $-V_w$ and $-V_r$ levels are maintained for a duration corresponding to the **ENABLE** pulse and the **SR** signals. The **VCOL** and **I** signals show a transition from $-V_w$ to $-V_r$ during the **ENABLE** period.

FIG. 6

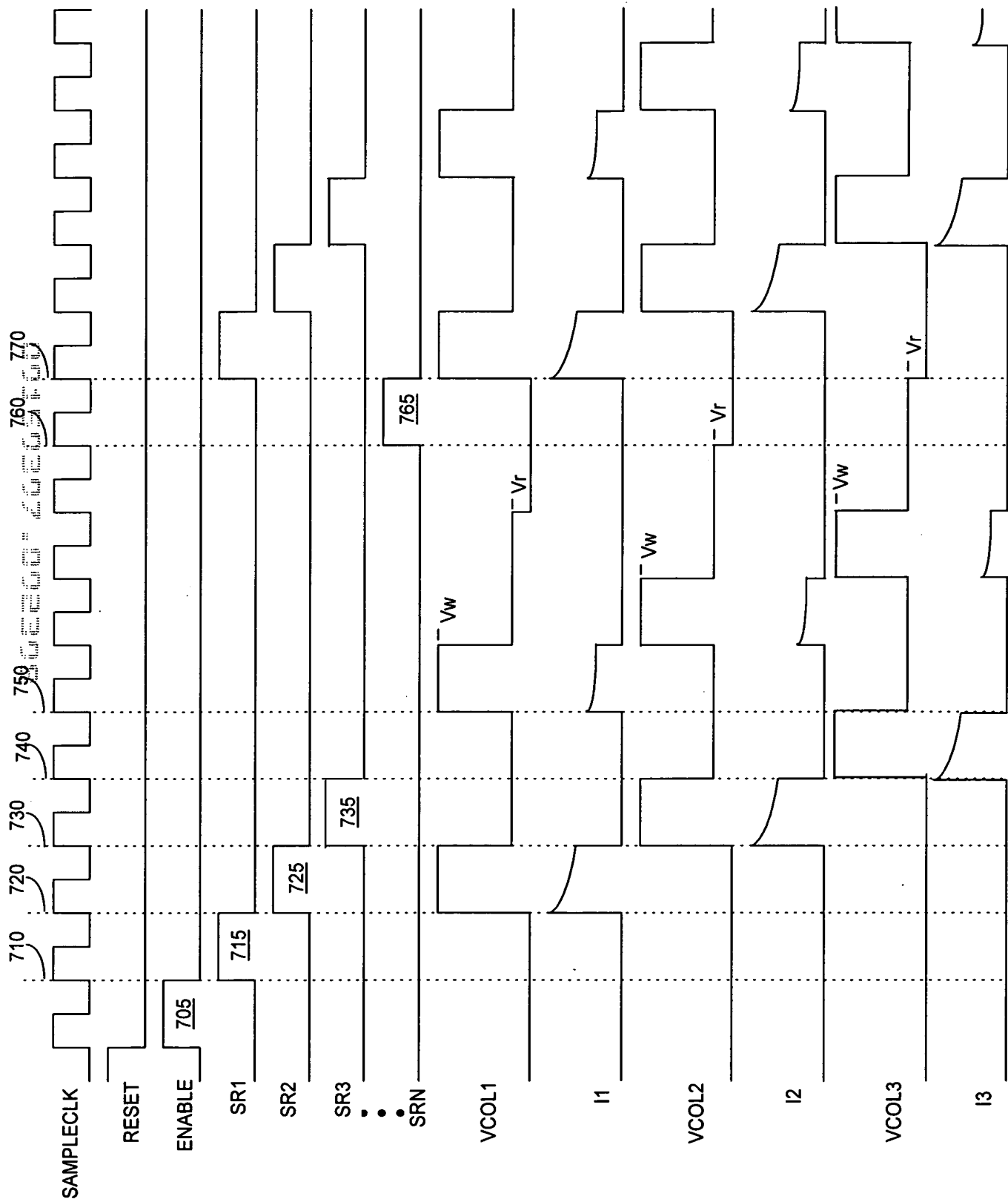


FIG. 7

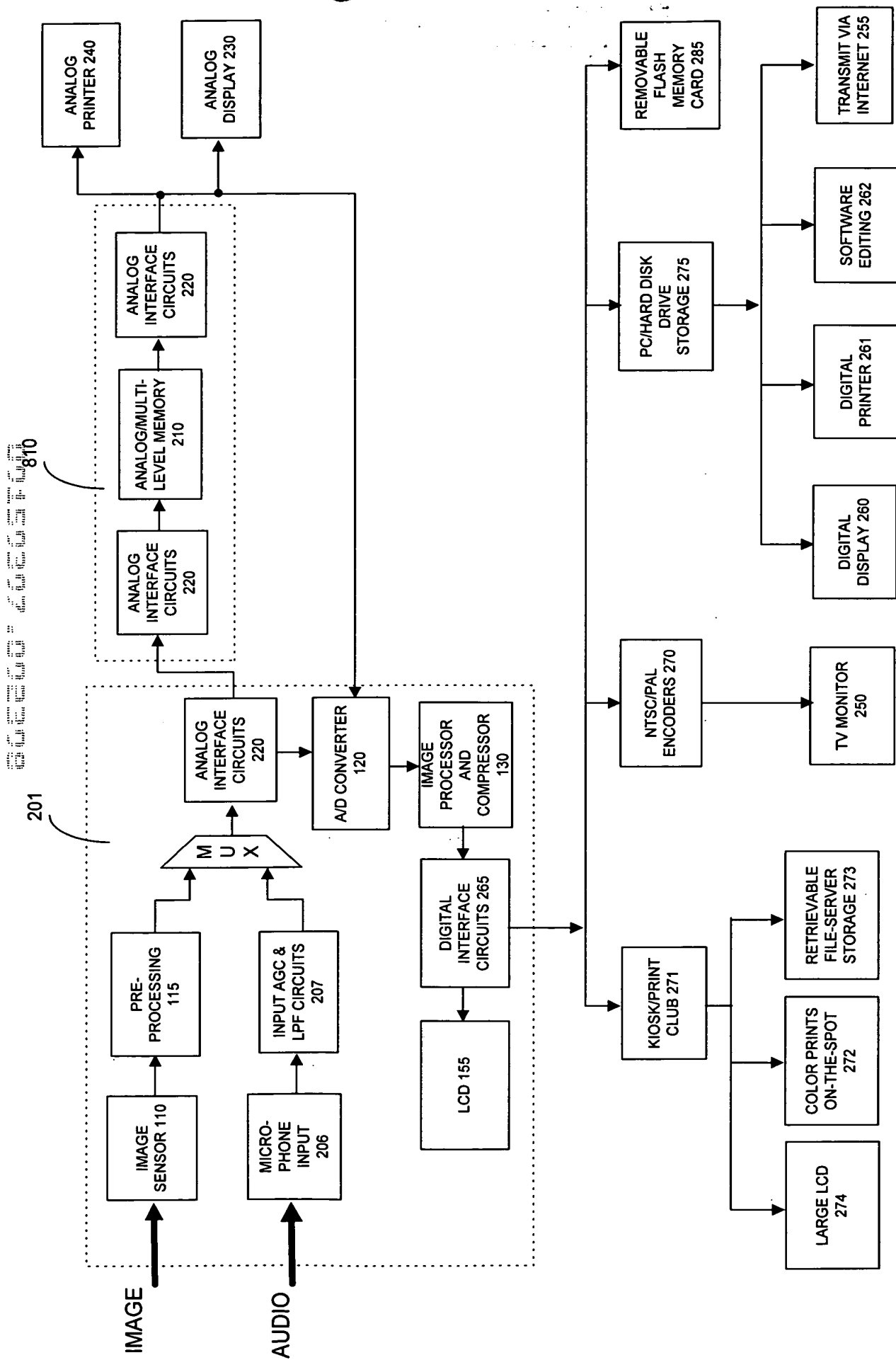


FIG. 8

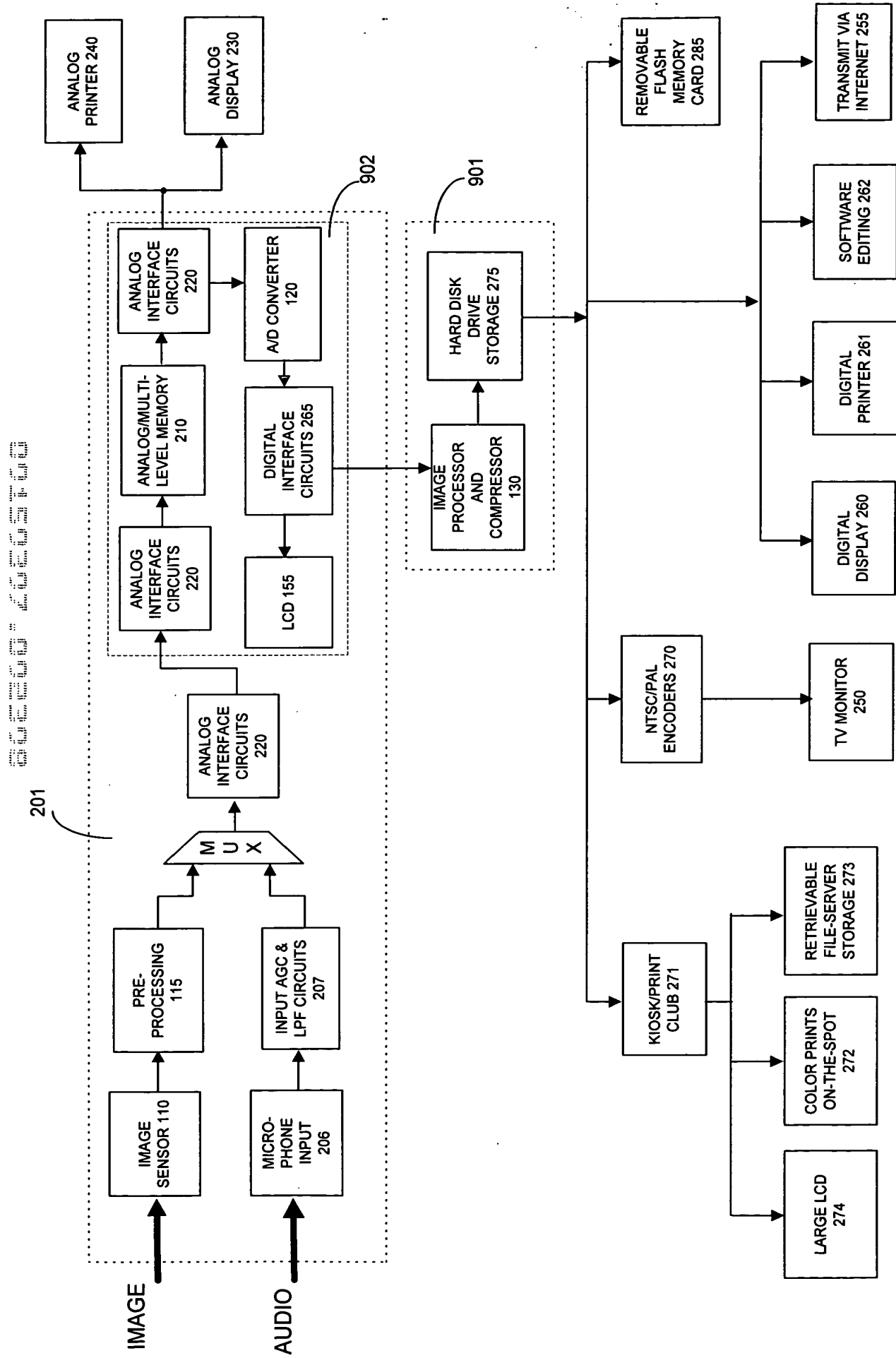


FIG. 9

